A 1V Ultra-Low Power High Precision CMOS Voltage Reference

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Abstract – A 1V ultra-low power high precision voltage reference is designed and implemented with UMC mixed-signal 0.18-um CMOS technology. A novel low-voltage high-precision current mirror is introduced in the voltage reference in order to reduce temperature coefficient and line regulation. Post simulation results show that the reference voltage and total power dissipation are 406.5mV and 0.83uW, respectively. Temperature coefficient of the voltage reference is 18.5ppm/°C when temperature ranges from −45°C to 90°C, while line regulation is 1%/V when the supply voltage ranges from 1V to 2.4V. The circuit layout occupies approximately 106um×81um.

I. INTRODUCTION

Voltage reference circuit is important in analog systems and mixed-signal integrated systems because it is responsible for generating stable voltage reference (Vref) that is insensitive to the variation of temperature and voltage supply (VDD). Traditional voltage reference combines a PTAT (proportional to absolute temperature) voltage and a CTAT (complementary to absolute temperature) voltage to generate a silicon bandgap voltage (around 1.25V) that is independent of temperature. In low power voltage reference circuit with supply voltage below 1.25V, traditional Vref design method is not applicable. Using current mode and resistive subdivision could generate a Vref below 1V [2, 3], but this method not only needs bipolar junction transistor (BJT), which requires additional fabrication steps in standard CMOS technology, but also needs large resistance in parallel with BJT to reduce current, which will increase silicon area.

Because of the drawbacks of design methods mentioned above, CMOS low voltage low power voltage reference is drawing increasingly more attention in recent years. Although a stable Vref could be obtained using zero temperature coefficient (ZTC) bias [4], the several tens of microwatts power dissipation makes the ZTC method unsuitable for low power applications. Another method takes advantage of the different temperature characteristic between PMOSFET and NMOSFET to realize temperature independent Vref [5], but unfortunately, this Vref is sensitive to the variation of VDD. Using self-biasing circuit could obtain Vref insensitive to the variation of VDD variation [6, 7], but as traditional cascode current mirror (CM) could not be applied under low VDD condition, the current copy error (CCE) of the CM in [6, 7] could not be reduced effectively, and thus precision of the Vref is not satisfactory.

This paper is organized as follows. A low voltage high precision CM is introduced in Section II, and a voltage reference based on this CM is analyzed in Section III. Section IV shows the post simulation results.

II. LOW VOLTAGE HIGH PRECISION CM

This section describes the circuit in [6], analyzes why the CM precision is the bottleneck of this circuit, and proposes a novel low voltage high precision CM.

A. CMOS voltage reference in [6]

The circuit in Fig. 1 consists of Start-up, IPTAT Generator, IGS Generator and I-V Convertor.

1) IPTAT Generator

M1 and M2 both operate in sub-threshold region and their drain currents follow:

\[ I_D = I_{D0} S e^{\frac{V_{GS} - V_T}{S}} \]

where \( V_{GS}, V_{th} \) and \( V_{DS} \) are the MOSFET gate-source, threshold and drain-source voltages respectively, \( V_T=kT/q \) is the thermal voltage, \( n \) is the slope factor, \( S=W/L \) is the MOSFET aspect ratio and \( I_{D0} \) is the drain current under the condition \( V_{GS}=V_{th} \) and \( S=1 \). If \( V_{DS}=4V_T \), (1) can be approximated as:

\[ I_D \approx I_{D0} S e^{\frac{V_{GS} - V_{T}}{S}} \]

(2)

M3 and M4 both operate in saturation region and have the same size, so the current through R1 could be expressed as:

\[ I_{PTAT} = I_{R1} = V_{GS2} - V_{GS1} \approx n \frac{V_T}{R_1} \ln \left( \frac{S_1}{S_2} \right) \]

(3)

2) IGS Generator

M5 operates in sub-threshold region, and thus

\[ I_{DS} \approx I_{PTAT} \left( \frac{S_1}{S_2} \right) \approx I_{D0} S e^{\frac{V_{GS} - V_{T}}{S}} \]

(4)

\[ V_{GS} = V_{th} + nV_T \ln \left( \frac{I_{DS}}{I_{D0} S} \right) \]

(5)

In (5), \( I_{DS} \) is much lower than \( I_{D0} S \) as M5 operates in sub-threshold region. Therefore, \( V_{GS} \) will decrease when temperature rises and consequently, current through \( R_2 \) is of CTAT characteristic [6].
3) I-V Converter PTAT current and CTAT current are summed after mirrored by M10 and M11, thereby generating $V_{ref}$ insensitive to temperature variation.

Fig. 1. CMOS voltage reference in [6]

B. Analysis of the circuit architecture in [6]

1) $I_{PTAT}$ Generator is the key module This module not only supplies PTAT current, but also provides bias current to M5, whose $V_{DS}$ is imposed on R3 to generate CTAT current in $I_{GS}$ Generator. Thus, the precision of $I_{PTAT}$ determines the precision of $V_{ref}$.

2) CCE influences line regulation of $V_{ref}$. When $V_{DD}$ changes to $V_{DD} + \Delta V$, $V_{DS1}$ is approximately unchanged, while $V_{DS4}$ changes to $V_{DS4} + \Delta V$. Considering channel length modulation effect, CCE of the CM composed of M3 and M4 causes $I_{DS4}$ not equal to $I_{DS2}$. Likewise, when $V_{DD}$ changes to $V_{DD} + \Delta V$, $V_{DS2}$ is approximately unchanged, while $V_{DS1}$ changes to $V_{DS1} + \Delta V$. Rewrite (3) as:

$$I_{PTAT} = \frac{nV_{T}}{R_{i}} \ln \left( \frac{S_{I_{DS4}} V_{DS4}}{S_{I_{DS2}} V_{DS2}} \right)$$

and it is clear that because of CCE of the CM in $I_{PTAT}$ Generator, $V_{DD}$ influences $I_{PTAT}$, and consequently $V_{ref}$.

3) CCE influences TC of $V_{ref}$. The ratio of the input current to the output current is not necessarily equal to the ratio of the input MOSFET size to the output MOSFET size because of CCE of the CM in I-V Converter, so TC of the $V_{ref}$ in [6] is not low enough.

C. Methods to reduce CCE in $I_{PTAT}$ Generator

Fig. 2(a) exhibits an ideal $I_{PTAT}$ Generator. When $V_{DD}$ changes to $V_{DD} + \Delta V$, $V_{sd}$ and $V_{ns}$ is unchanged due to the ideal characteristic of module A and B, while $V_{sd}$ and $V_{ns}$ changes to $V_{sd} + \Delta V$ and $V_{ns} + \Delta V$ respectively. As a result, $I_{PTAT}$ could be expressed by (3) precisely. In practice, module A and B could not have ideal characteristic and thus, CCE of CM could only be reduced as small as possible.

Several strategies could be used to reduce CCE. One strategy uses the virtual short property of operational amplifier to obtain the same voltage at n1 and n2, but CCE caused by $V_{sd}$-$V_{ns}$ still exists. Another strategy is to substitute PM1, PM2, NM1 and NM2 with cascode structure, but the minimum $V_{DD}$ required is $V_{GSN} + V_{DSN} + V_{GPS} + V_{SDP}$, which is hardly reached when $V_{DD}$ is reduced to 1V. Fig.2. (b) shows an $I_{PTAT}$ Generator that uses level shifting structure as its key element. Module C senses the voltage variation at n2, and $V_{sd}$ will follow $V_{ns}$ under the effect of source follower PM3. Likewise, $V_{sd}$ will follow $V_{ns}$. According to (6), CCE will be reduced greatly.

Fig. 2. $I_{PTAT}$ Generator: (a) Ideal scheme (b) the scheme using level shifting structure

Fig. 3 shows a transistor level implementation of an $I_{PTAT}$ Generator using a novel low-voltage high-precision CM, where:

$$S_{PM1} = S_{PM2} = S_{PM3} = S_{PM4}$$
$$S_{NM1} = S_{NM4}, S_{NM2} = S_{NM5}$$
$$S_{PM3} = S_{PM6}, S_{NM3} = S_{NM6}$$
$$R_{0} = R_{i}$$

Ignoring the high order effects, the current through $R_{0}$ and $R_{i}$ could both be expressed as (3) and the nodal voltages satisfy:

$$V_{e1} \approx V_{e2}, \quad V_{SG,PM6} \approx V_{SG,PM3}$$
$$V_{e7} \approx V_{e3}, \quad V_{GS,NM6} \approx V_{GS,NM3}$$

Due to the level shifting process in (8), no matter how $V_{DD}$ changes, the following relations will still be satisfied:

$$V_{e1} \approx V_{e2}$$
$$V_{e3} \approx V_{e4}$$

and the level shifting characteristic of the scheme in Fig. 2(b) is achieved.

Fig. 3. Proposed $I_{PTAT}$ Generator using a novel low-voltage high-precision CM

III. THE WHOLE CIRCUIT OF THE PROPOSED VOLTAGE REFERENCE

A. Principle of the circuit

Fig. 4 shows the whole circuit of the proposed voltage reference, which contains:
1) Start-up

When the circuit is powered on, \(V_{DD}\) injects pulse currents through PM18 and PM19 to set \(I_{PTAT}\) circuit to the right operating point.

2) \(I_{PTAT}\) Generator

To reduce the voltage margin consumption, all MOSFETs are operated in sub-threshold region, and in this condition, the minimum \(V_{DD}\) required is \(V_{GSP}+V_{GSN}+|V_{DS}|\). \(I_{PTAT}\) could be expressed as:

\[
I_{PTAT} = I_{R0} = \frac{nV_T}{R_i(T)} \ln \left( \frac{S_{NM2}}{S_{NM1}} \right) \quad (10)
\]

Here, temperature characteristic of the resistance is considered:

\[
R_i(T) \approx R_i(T_0) \left[ 1 + TC_i \left( T - T_0 \right) \right], \quad i = 0, 1, 2, 3 \quad (11)
\]

in which \(TC_i \approx -0.8m\) is the first order temperature coefficient of the N-Well resistance used in this design.

3) \(I_{CTAT}\) Generator

To reduce the CCE of the CM composed of PM7 and PM2, the sizes of PM7 and PM8 should satisfy:

\[
\frac{S_{PM7}}{S_{PM2}} = \frac{S_{PM8}}{S_{PM6}} \quad (12)
\]

NM7 operating in sub-threshold region has big aspect ratio (80u/2u) to achieve two goals: a) as the current through NM7 is determined by \(I_{PTAT}\), big aspect ratio means small \(V_{GS,NM7}\), and accordingly, small \(R_2\) on the condition that the \(I_{CTAT}\) is given; b) the relationship between \(V_{GS}\) and temperature is [7]:

\[
V_{GS}(T) \approx V_{GS}(T_0) + K_G \left( \frac{T}{T_0} - 1 \right) \quad (13)
\]

where

\[
K_G \equiv K_T + V_{GS}(T_0) - V_{th}(T_0) - V_{OFF} \quad (14)
\]

Here, \(K_T \approx -0.2\) is the TC of \(V_{th}\) under the UMC 0.18um technology and \(V_{OFF}\) is a constant in BSIM3v3. According to (13) and (14), if \(V_{GS}(T_d) < V_{th}(T_d), V_{GS}(T)\) exhibits CTAT characteristic:

\[
I_{CTAT} = \frac{V_{GS,NM7}(T_0) + K_G \left( \frac{T}{T_0} - 1 \right)}{R_s(T)} \quad (15)
\]

In addition, CCE of the CM composed of PM9 and PM11 could be reduced by tuning the sizes of NM8, NM9, PM12 and PM10 to make \(V_{n10}\) follow \(V_{n9}\).

4) \(V_{ref}\) Output

CCE of the CM composed of PM2 and PM15 and CCE of the CM composed of PM9 and PM13 could both be reduced by level shifting. According to (10) and (15), the output \(V_{ref}\) follows:

\[
V_{ref} = R_s(T) \left[ \frac{nV_T}{S_{PM15}} \right] + \frac{nV_T}{R_i(T)} \ln \left( \frac{S_{NM2}}{S_{NM1}} \right) + \frac{S_{PM13}}{S_{PM9}} \left[ V_{GS,NM7}(T_0) + K_G \left( \frac{T}{T_0} - 1 \right) \right] \quad (16)
\]

Fig. 4. The whole circuit of the proposed voltage reference

B. Layout of the voltage reference

This voltage reference is designed with UMC 0.18um mixed signal technology and layout of the whole circuit occupies 106um×81um.

Fig. 5. Layout of the proposed voltage reference

IV. POST SIMULATION RESULTS

A. Temperature coefficient

Temperature coefficient (TC) is defined as:

\[
TC = \frac{1}{V_{ref}} \left[ \frac{V_{ref(MAX)} - V_{ref(MIN)}}{T_{(MAX)} - T_{(MIN)}} \right] \times 10^6 \quad (17)
\]

Fig. 6 shows the temperature characteristic of \(V_{ref}\). When temperature range is \([-45^\circ C, 90^\circ C]\), the TC of \(V_{ref}\) under different \(V_{DD}\) is shown in Table 1. From practical perspective, only the \(V_{ref}\) with the \(V_{DD}\) lower than 2.4V is provided.

Fig. 6. Temperature characteristic of \(V_{ref}\)
Table I

TC OF $V_{REF}$ UNDER DIFFERENT $V_{DD}$

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>1.0</th>
<th>1.2</th>
<th>1.4</th>
<th>1.6</th>
<th>1.8</th>
<th>2.0</th>
<th>2.2</th>
<th>2.4</th>
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<tbody>
<tr>
<td>TC (ppm/℃)</td>
<td>18.5</td>
<td>18.3</td>
<td>18.3</td>
<td>18.0</td>
<td>17.8</td>
<td>17.5</td>
<td>17.1</td>
<td>16.8</td>
</tr>
</tbody>
</table>

B. Line Regulation and total power

Line regulation is defined as:

$$\text{Line regulation} = \frac{V_{ref(MAX)} - V_{ref(MIN)}}{V_{DD(MAX)} - V_{DD(MIN)}}$$

As Fig. 7 shows, the line regulation of $V_{ref}$ is 1%/V when $V_{DD}$ ranges from 1V to 2.4V and the total power is 0.83uW when $V_{DD}$ is 1V.

Fig. 7 Output $V_{ref}$ and total power under different $V_{DD}$

C. Performance comparison with [6] and [7]

According to Table II, the proposed voltage reference has the lowest power dissipation and highest precision compared with the reference in [6] and [7], although all three references base on similar principle.

Table II

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Paper[6]*</th>
<th>Paper[7]*</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process (um)</td>
<td>0.09</td>
<td>1.2</td>
<td>0.18</td>
</tr>
<tr>
<td>$V_{DD}$ (min) (V)</td>
<td>1</td>
<td>1.2</td>
<td>1</td>
</tr>
<tr>
<td>$I_{ref}$ (μA)</td>
<td>1.3</td>
<td>4</td>
<td>0.83</td>
</tr>
<tr>
<td>$T$ range (℃)</td>
<td>−20−90</td>
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<td>$TC$ (ppm/℃)</td>
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<td>71.4</td>
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<tr>
<td>Line regulation (%/V)</td>
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<td>—</td>
<td>1</td>
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<tr>
<td>Area (mm²)</td>
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<td>0.008</td>
</tr>
</tbody>
</table>


V. CONCLUSION

A novel ultra low voltage high precision current mirror is proposed, and a CMOS voltage reference based on it is designed. This voltage reference is designed and implemented with UMC mixed-signal 0.18-um CMOS technology. Post simulation shows that when $V_{DD}$ is 1V and temperature is 27℃, the total current equals 0.83uA, the output $V_{ref}$ equals 406.5mV and TC of $V_{ref}$ equals 18.5ppm/℃ when temperature ranges from −45℃ to 90℃. Line regulation of $V_{ref}$ is 1%/V When $V_{DD}$ ranges from 1V to 2.4V. The circuit layout occupies approximately 106um×81um. This voltage reference is suitable for micro-power electronic applications such as biochip and wireless communication system.

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REFERENCES