Full Custom Design of a Three-Stage Amplifier with 5500MHz·pF/mW Performance in 0.18μm CMOS

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Abstract—A full custom design of a three-stage amplifier is described in this paper. A feedback transconductance stage and a feedforward stage combined with two Miller compensation capacitors are used for frequency compensation. The circuit is designed in 0.18μm CMOS process with a 1.8V supply voltage. When driving a 150pF capacitive load, the amplifier achieves over 100dB dc gain, 2.24MHz gain-bandwidth product (GBW), 62° phase margin (PM), 1.2V/μs slew rate (SR) and 61μW power dissipation. Compared to conventional multistage amplifiers, this work provides improvement in both GBW and SR, and also shows a significant improvement in MHz·pF/mW performance.

I. INTRODUCTION

The supply voltage of the VLSI continuously scales down with advanced deep sub-micrometer technologies. Low supply voltage and low power electronic system becomes the main design challenge for many applications. The operational amplifier (OPA), which is needed in almost all analog and mixed-signal systems, has to keep up with the fast advances in present-day process. However, single-stage or two-stage amplifiers based on cascoding transistors are no longer suitable for low supply voltages. In order to achieve high gain and comparatively higher output voltage swing, a multistage amplifier is widely used by increasing the number of gain stages horizontally. Nonetheless, all multistage amplifiers suffer from the closed-loop stability problem since high-resistance nodes between the stages generate poles and zeros with the parasitic capacitances, which can greatly interfere with frequency response. Thus a multistage amplifier must be frequency compensated in order to either cancel the redundant poles and zeros or shift them to higher frequency range.

Several frequency compensation topologies for multistage amplifiers are reported [1]-[6]. The nested Miller compensation (NMC) is well known to split the poles so the nondominant poles can be shifted to higher frequency than unity-gain frequency [1]. The structure of NMC is depicted in Fig. 1. Parameters g_{m}, r, and C_{p} are transconductance, output resistance and parasitic capacitance for the i-th stage, respectively. C_{l} stands for the load capacitance, and C_{m1} and C_{m2} are compensation capacitors. Careful scrutiny on this topology reveals that the Miller capacitor C_{m2} is a serious source of instability since the phase shift reaches 180° with the increase of frequency. As a result, extra power is required to ensure stability. Since the first and second nondominant pole p_{n1} and p_{n2} is often required to be above 3 and 5 times of Gain-Bandwidth Product, g_{m2} and g_{m3} are given by

\[
g_{m2} \geq 6\pi \cdot GBW \cdot C_{m2}, \quad (1)
\]
\[
g_{m3} \geq 10\pi \cdot GBW \cdot C_{l}. \quad (2)
\]

The NMC topology is not suitable for low power applications since the required transconductance is 5 times the transconductance for single stage amplifier.

Many frequency compensation topologies are based on NMC structure, such as multipath nested Miller compensation (MNMC) [1], nested G_{m}-C compensation (NGCC) [2], and NMC with feedforward transconductance stage and nulling resistor (NMCFNRR) [3]. Some other advanced topologies have been proposed to improve bandwidth, such as Damping-factor control frequency compensation topology (DFCFC) [4], positive-feedback compensation topology (PFC) [5], active-feedback frequency compensation (AFFC) [6] and transconductance with capacitances feedback compensation (TCFC) [7].

In this paper, a full custom design of a three-stage CMOS amplifier based on TCFC is described with high figure of merit (FOM) defined as

\[
\text{FOM}_{S} = \frac{\text{GBW} \cdot C_{l}}{\text{power}}.
\]
\[
\text{FOM}_{I} = \frac{\text{SR} \cdot C_{l}}{\text{power}}.
\]

The frequency compensation structure includes a transistor to provide feedback transconductance and a feedforward stage. The feedback transistor attenuates the feedforward
signal, and the feedforward stage is used to form a Class-AB output stage so as to provide large slew rate. In addition, this amplifier can be used to drive large capacitance load and it occupies low die area.

II. ADOPTED COMPENSATION TECHNIQUE

A. Topology and Transfer Function

The adopted frequency compensation structure is depicted in Fig. 2. Compensation exploits \( C_{m1}, C_{m2}, \) a feedback transistor \( M_a \) and an active transconductance stage. The parameters shown in Fig. 2 are the same as defined before. Here \( g_{mf} \) represents the transconductance of the feedforward stage, and \( 1/g_{ma} \) is output resistance of transistor \( M_a \). For simplification, we assume the dc gain of each stage is much larger than 1, and \( C_{m1} \) and \( C_{m2} \) are much larger than parasitic capacitors \( C_{pi} \), and \( C_L \) is much larger than \( C_{m1} \) and \( C_{m2} \). Thus, the small-signal transfer function of the open-loop gain can be expressed by (4). From (4), we can get dc gain \( A_{dc} \), the dominant pole \( p_{-3dB} \) and GBW as

\[
A_{dc} = g_{mf} g_{m2} g_{m3} r_2 r_3
\]

\[
p_{-3dB} = \frac{1}{g_{ma} g_{m2} g_{m3} r_2 r_3}
\]

\[
GBW = A_{dc} \cdot p_{-3dB} = \frac{g_{mf}}{C_{m1}}.
\]

Notice that \( g_{mf} \) does not appear in the denominator of the transfer function. Thus the feedforward stage does not introduce any poles and it helps to improve slew rate of the amplifier.

B. Stability Analysis and GBW

The stability condition of the adopted structure can be studied by first neglecting the zeros in (4). Actually, there is a left half plane (LHP) zero. The close-loop transfer function \( A_{cl}(s) \) of the amplifier connected as in unity-gain feedback configuration can be derived as (8). As the order of the numerator in (8) is less than that of the denominator, the stability is determined by the denominator. Routh stability criterion can be used to evaluate system stability conditions [2], and it reveals that the amplifier is stable if

\[
2\pi GBW < \frac{C_{m2}}{C_{p2}} \cdot \frac{g_{mf}}{C_L}.
\]

By comparing the coefficients of the denominators of (8) with those of (10), we can get

\[
\frac{C_{m1}}{g_{mf}} = \frac{2.613}{\omega_0}
\]

\[
\frac{C_{m1} C_{m2}}{g_{mf} S_{m2}} (1 + \frac{g_{mf}}{g_{mf}}) = \frac{3.414}{\omega_0^2}
\]

\[
\frac{C_{m1} C_{m2} C_{p2} C_L}{g_{mf} S_{m2} S_{m3}} = \frac{2.613}{\omega_0^2}
\]

\[
\frac{C_{m1} C_{m2} C_{p2} C_L}{g_{mf} S_{m2} S_{m3} S_{m4}} = \frac{1}{\omega_0^4}.
\]

C. Dimension Conditions

The stability of the adopted structure can also be achieved when the denominator of the close-loop transfer function (8) has a fourth-order Butterworth polynomial \( B(s) \) with a cutoff frequency of \( \omega_0 \), which is given by

\[
B(s) = 1 + 2.613 s + 3.414 s^2 + 2.613 s^3 + s^4.
\]

The dimension conditions of \( C_{m2} \) can be deduced from (12)–(14) and eliminating \( \omega_0 \). This can be written as

\[
A(s) = \frac{1}{1 + \frac{r_1 r_2 r_3 g_{mf} g_{m2} g_{m3}}{g_{mf} S_{m2} S_{m3}}} \left[ \frac{1 + \frac{C_{m2}}{g_{mf}} - \frac{C_{m1} C_{p2}}{g_{mf} S_{m3}} - \frac{C_{m2} C_{p2}}{g_{mf} S_{m3}} g_{mf} S_{m4} / g_{mf} S_{m2}}{g_{mf} S_{m2} S_{m3}} \right] \frac{C_{m1} C_{p2} C_L}{g_{mf} S_{m2} S_{m3}} S^3.
\]

\[
A_{cl}(s) = \frac{1}{1 + \frac{C_{m1}}{g_{mf}} + \frac{C_{m1} C_{m2}}{g_{mf} S_{m2} S_{m3}} (1 + \frac{g_{mf}}{g_{mf}}) + \frac{C_{m1} C_{p2} C_L}{g_{mf} S_{m2} S_{m3}} + \frac{C_{m2} C_{p2} C_L}{g_{mf} S_{m2} S_{m3} S_{m4}}}.
\]
Fig. 3. Circuit schematic of a three-stage amplifier.

\[
C_{m1(NMC)} = \frac{2g_{m1}C_{m1}L}{g_{m2}(g_{m2} + g_{m3})}, \quad \text{(17)}
\]

Where

\[
N = \frac{50g_{m1}^2(1 + g_{m2})C_{m1}}{g_{m2}}, \quad \text{(16)}
\]

And

\[
C_{m1(NMC)} = \frac{5g_{m1}C_{m1}L}{g_{m2}}, \quad \text{(18)}
\]

\(C_{m1(NMC)}\) stands for the compensation capacitor \(C_{m1}\) in the NMC structure. Since \(C_{m1}\) is much larger than \(C_{m2}\), the size of \(C_{m2}\) in the adopted structure is much smaller than \(C_{m1(NMC)}\) as \(N \gg 1\). Also, the dimension conditions of \(C_{m1}\) can be deduced from (11)–(12) as

\[
C_{m1} = \frac{2g_{m1}C_{m1}(g_{m2} + g_{m3})}{g_{m2}}, \quad \text{(18)}
\]

(18) reveals that \(C_{m1}\) has similar size as \(C_{m2}\), and it is much smaller than \(C_{m1(NMC)}\). Thus, the adopted topology occupies much less die area than NMC structure because the compensation capacitors need not to be very large.

D. Phase Margin

From the open-loop transfer function in (4), the first nondominant pole \(p_{nd1}\) and the LHP zero \(z_1\) are given by

\[
p_{nd1} = -\frac{g_{m1}g_{m2}}{(g_{m2} + g_{m3})C_{m2}}, \quad \text{(19)}
\]

\[
z_1 = -\frac{g_{m1}g_{m2}}{C_{m2}g_{m2}}p_{nd1}. \quad \text{(20)}
\]

Both \(p_{nd1}\) and zero \(z_1\) are independent of imprecise parasitic capacitors. Other nondominant poles and zeros are much larger so their effects on phase margin can be neglected. The overall phase margin (PM) is given by

\[
\text{PM} = 90^\circ - \arctan \left(\frac{2\pi GBW}{|p_{nd1}|}\right) + \arctan \left(\frac{2\pi GBW}{|z_1|}\right). \quad \text{(21)}
\]

Since \(z_1\) is slightly larger than \(p_{nd1}\), the phase margin can be improved by the LHP zero.

E. Slew Rate

With the feedforward stage \(g_{mf}\), the last stage of the amplifier becomes a Class-AB output stage which slews fast in both directions. Thus the first stage which drives the \(C_{m1}\) becomes the dominant limitation of the overall SR, which is given by

\[
\text{SR} = \frac{I_{stage1}}{C_{m1}}, \quad \text{(22)}
\]

Where \(I_{stage1}\) stands for the current of the first stage.

F. Low-Power Design Considerations

The stability conditions require the NMC amplifier has large transconductance of the last stage, i.e. \(g_{m3} \gg g_{m1}\), thus it is not suitable for low-power applications. The adopted structure is desirable for low-power design because the transconductance of the output stage need not be too large. This can be deduced from (9) as

\[
g_{m3} > \frac{2\pi \cdot \text{GBW} \cdot C_{m2} g_{m2}}{C_{m2}}, \quad \text{(23)}
\]

Where \(g_{m3(s\text{ingle})}\) represents for the transconductance of a single stage amplifier. \(g_{m2}\) can be small since \(C_{m2}\) is much smaller than \(C_{m1}\).
The biasing network schematic is shown in Fig. 4. Ib is the input reference current which generates the biasing voltages. Transistors Mb1-Mb8 work at saturation region to generate vb1-vb5.

The transistor size is designed to achieve following specifications: Open-loop gain above 120dB, SR larger than 1V/μs, power less than 80μW, GBW more than 1.5MHz, PM more than 50°. These specifications reveal that the amplifier has a FOMs above 2813MHz·pF/mW, and FOML above 1875V·pF/μs/mW. This shows that the amplifier has high performance since it has high FOM value. Much design effort is put on further optimizing the FOM value.

The circuit parameters of the amplifier are shown in Table I. The amplifier is designed in a 0.18μm CMOS process and the supply voltage is 1.8V. The capacitors used to compensate frequency response are implemented by metal-insulator-metal (MIM) capacitors. This process is compatible with most VLSI systems. In addition, the stability is insensitive to the absolute value of the compensation capacitors.

IV. SIMULATION RESULT AND LAYOUT

The three-stage amplifier is simulated with a 150pF capacitive load. The frequency response of the amplifier has been tested with input common-mode voltage of 800mV, and the transient response together with SR have been tested when the amplifier is connected in unity-gain with a 1V step input. The simulation result of frequency and transient response are shown in Fig. 5 and Fig. 6, respectively. From Fig. 5, the amplifier achieves a GBW of 2.241MHz, a dc Gain of 134.7dB and a PM of 62°. From Fig. 6, the SR- and SR+ are 1.16V/μs and 1.23V/μs, respectively. The results are summarized in Table II. The design specifications are well satisfied.

A. Circuit Robustness Analysis

In actual electronic systems, nonideal factors may deteriorate the circuit performance especially for the analog system. In this design, we mainly consider how the fluctuation of supply voltage Vdd and biasing current Ib affect the FOMs value, which reflects the performance of frequency response and power dissipation. The relationship among FOMs, Vdd, and Ib are illustrated in Fig. 7 within different environment temperature. Assuming that Vdd fluctuates between 1.6V and 2.1V, Ib fluctuates between 25μA and 35μA. In addition, different technology corners are considered during the simulation, including typical NMOS with typical PMOS (TT); fast NMOS with fast PMOS (FF); slow NMOS with slow PMOS (SS); slow

<table>
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<tr>
<th>Parameter</th>
<th>Specifications</th>
<th>Simulation Value</th>
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<tr>
<td>DC Gain</td>
<td>&gt;100 dB</td>
<td>134.7 dB</td>
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<tr>
<td>Gain-bandwidth Product</td>
<td>&gt;1.5MHz</td>
<td>2.241 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>&gt;50°</td>
<td>62°</td>
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<td>Vdd</td>
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<tr>
<td>Ib</td>
<td>&lt;45 μA</td>
<td>33.8 μA</td>
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<tr>
<td>Power</td>
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<td>60.9 pW</td>
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<tr>
<td>Slew Rate +/-</td>
<td>&gt;1 V/μs</td>
<td>1.16/1.23 V/μs</td>
</tr>
<tr>
<td>Settling Time +/- (to 1%)</td>
<td>–</td>
<td>2.93/1.72 μs</td>
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NMOS with fast PMOS (SNFP) and fast NMOS with slow PMOS (FNSP). The simulation results reveal that the FOMs value is insensitive to Vdd and Ib fluctuation and also the temperature, and it keeps well between 5000-6500 MHz·pF/mW, which is a desirable value. The same analysis can be applied to FOMp, which also reflects the robustness of the amplifier. From Fig. 7 (a)-Fig. 7 (c), the FOMs value increases when Vdd and Ib decreases, or the temperature goes down within a certain range. Fig. 8 shows the phase margin range in different Vdd, Ib, technology corner and input common mode voltage conditions, where input common mode voltage ranges from 0.2V to 0.8V. From Fig. 8, the PM stays well between 51° and 66°, which guarantees stability of the amplifier. The comparison results of this work and previous reports are given in Table III. The simulation result prevails over most previous topologies. The FOM value is not as good as TCFC report since this work is designed in 0.18μm technology process.

Fig. 7. The relationship among FOMs, Vdd, and Ib
(a) T = 0℃ (b) T = 27℃ (c) T = 50℃.

Fig. 8. Phase Margin in different conditions
(different Vdd, Ib, temperature, technology corner, input common mode voltage are considered).

| Table III. Comparison of different multistage amplifiers |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| CL (pF)        | 100            | 100            | 20             | 100            | 100            | 100            | 130            | 150            | 150             |
| DC Gain (dB)   | 100            | 100            | 100            | >100           | >100           | >100           | >100           | 100            | 135             |
| GBW (MHz)      | 60             | 100            | 0.61           | 1.8            | 2.6            | 2.7            | 4.5            | 2.85           | 2.24            |
| Phase Margin (degree) | 70       | 70             | 60             | 51             | 43             | 52             | 65             | 58.6           | 62              |
| Vdd (V)        | 8.0            | 8.0            | 2.0            | 2.0            | 2.0            | 1.5            | 2.0            | 1.5            | 1.8             |
| Power (mW)     | 76             | 76             | 0.68           | 0.41           | 0.42           | 0.275          | 0.40           | 0.045          | 0.061           |
| Slew Rate (V/μs) | 20            | 35             | 2.5            | 0.79           | 1.32           | 1.0            | 1.49           | 1.035          | 1.20            |
| FOMs (MHz·pF/mW) | 79             | 132            | 18             | 443            | 619            | 1276           | 1350           | 9500           | 5500            |
| FOMp (V·pF/μs·mW) | 26             | 46             | 74             | 195            | 314            | 473            | 447            | 3450           | 2950            |

Technology
- 3GHz fT, BJT
- 3GHz fT, CMOS
- 2μm, 0.8μm, CMOS
- 0.8μm, 0.35μm, CMOS
- 0.8μm, 0.35μm, CMOS
- 0.18μm, CMOS

Average value is used
B. Layout

The layout of the amplifier including gain stages and biasing network is depicted in Fig. 9. The active area for the amplifier is about 0.03mm². In order to reduce mismatch, several dummy transistors are also included in the layout.

V. CONCLUSION

A full custom design of a three-stage amplifier is presented in this paper. We adopt a frequency compensation topology with a feedback transconductance stage and a feedforward stage combined with two Miller compensation capacitors. This topology improves the GBW and SR performance. In addition, the compensation capacitors are small compared to conventional topologies; thus the die area can be reduced. The amplifier achieves an overall FOM value of 5500MHz·pF/mW. It is desirable for low supply voltage and low power applications and is compatible with VLSI systems.

VI. ACKNOWLEDGEMENT

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