Power Analysis for the MOS AC/DC Rectifier of Passive RFID Transponders

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Abstract—The operating principle of MOS FETs AC/DC rectifier for passive RFID transponder is introduced and the power dissipation of MOS rectifier operating with 902M-928MHz industrial, scientific, and medical (ISM) carrier frequency is presented in details in this paper. In order to maximize the operating range of RFID transponder, low power design techniques are needed. Therefore, the key design parameters optimization of passive rectifier is discussed in this paper. Besides, the paper also discusses some design tradeoffs between area, power efficiency, communication bandwidth, the stability of output DC supply voltage.

I. INTRODUCTION

Rectifier, also called charge pump or voltage multiplier, converts input RF signal received by the antenna into a stable DC supply voltage for the analog frontend circuits, baseband DSP block and memory. Depending on the type of inputs, rectifier can be classified as AC/DC and DC/DC types [4]. This paper only focuses on the former. Rectifier is one of the essential parts of the RF interface circuits of RFID transponders. High sensitivity, low power rectifier is one of the most critical circuits of RFID transponder.

Typical AC/DC Rectifier circuit architecture used in common is composed of N-stage capacitor–diode network [2], as shown in Fig.1 [1]. This architecture is based on the DC/DC charge pump circuit, which is proposed by Dickson in 1976[3]. Owing to low series resistance, little threshold voltage, large saturation current and low Schottky junction capacitance, Silicon-Titantium Schottky diodes are generally used.

However, the particularity of manufacturing processes for Schottky diodes and the inconsistency in quality between different product processes often make the integration of Schottky rectifier incompatible with standard CMOS circuits and then limit its application [4]. So, various junction diodes, such as diode-connected MOS FETs, instead of the Schottky diodes are used in rectifier.

One of the main obstacles that restrict the development and the application of passive RFID transponder is the performance of RF rectifier. The primary index of it’s performance is the power efficiency and the stabilization of the output supply volta-
The N-Stage NMOS AC/DC rectifier.

er, we can use an approximately linear model to analyze [7]. Assumed that all transistors are identical, the output current is stable and all the coupling capacitor can be considered as short at the operating frequency, we analyze MOS AC/DC rectifier as follows.

A. The Operating Principle of N-stage rectifier (Neglecting the Parasitic Capacitor of Transistors)

The Nth stage unit rectifier cell is shown in Fig. 3 (a) and (b). $C_{H(N)}$ is the horizontal coupling capacitor, $C_{V(N)}$ and $C_{V(N-1)}$ is the vertical capacitor.

During the negative phase of input RF signal $V_{rf}$ indicated in Fig. 3 (a), when $V_{N-1} > V_{rf}$, the transistor $M_{2N-4}$ turns on, for $V_{N} < V_{rf}$ at this time, the transistor $M_{2N}$ turns off. The charge transfers from capacitor $C_{V(N-1)}$ to capacitor $C_{H(N)}$, at the end of this charging process, the transistor $M_{2N-4}$ turns off. When the input signal changes to the positive phase shown in Fig. 3 (b), the voltage of input signal increases, and $V_{K}$ increases also, when $V_{K} > V_{N}$, the transistor $M_{2N}$ turns on, the charging current $I_{K}$ flows from capacitor $C_{H(N)}$ to $C_{V(N)}$. At the end of this process, some charges on capacitor $C_{V(N-1)}$ have been transferred to capacitor $C_{H(N)}$.

For N-stage rectifier as shown in Fig. 2, in the dc analysis, all the transistors are connected in series, so the dc voltage between every transistor’s two terminals is given by

$$V_{dc} = \frac{V_{out}}{2N}$$

(2)

And in the RF analysis, all the coupling capacitors can be considered as short-circuits, therefore, all the diode-connected transistors are connected in parallel or antiparallel between the RF input. The ac voltage of every transistor is given by

$$V_{ac} = \pm V_{rf}$$

(3)

where the sign “+” is applied to transistors with an even subscript.

B. The Operating Principle of N-stage rectifier (Take Parasitic Effect into Account)

The analysis above doesn’t consider any parasitic effects. Because the input signal of rectifier is large signal, the amplitude is often up to several hundreds millivolts, all the transistors operate at large signal condition. The large signal equivalent model of diode-connected transistor is shown in Fig. 4 [5]. The sum of all parasitic capacitors at the terminal $K$, that is $C_{S(K)}$, is given by

$$C_{S(K)} = C_{RS(N-1)} + C_{BD(N)} + C_{GB(N)}$$

(6)

As indicated above, in the RF analysis, the voltage of terminal $K$ is $\frac{V_{NH}}{V_{rf}} + \frac{C_{H(N)}}{C_{S(K)}}$. So the ac voltage of every transistor is given by

$$V_{ac} = \pm \frac{C_{H(N)}V_{rf}}{C_{H(N)} + C_{S(K)}}$$

(7)

So, the voltage that drops across each transistor is given by

$$V_{t} = V_{dc} + V_{ac} = \pm C_{H(N)}V_{rf} \left( C_{H(N)} + C_{S(K)} \right) + \frac{V_{out}}{2N}$$

(8)

And the output voltage also changes to

$$V_{N} = 2N \left( \frac{C_{H(N)}V_{rf}}{C_{H(N)} + C_{S(K)}} - V_{d(evon)} \right)$$

(9)

The equation (9) shows that the larger the capacitance of parasitic capacitor $C_{S(K)}$ is, the lower of output voltage is. For the same output voltage and load, the amplitude of RF input should be increased. And the RF input power should be increased too. Therefore, the power efficiency will decrease. So

Figure 2. The N-Stage NMOS AC/DC rectifier.

Figure 3. (a) The Nth-Stage Rectifier during the Negative Phase of input RF signal and (b) The Nth-Stage Rectifier during the Positive phase of input RF signal. ($C_s(k)$ is the sum of all parasitic capacitors at the terminal $K$).
we should take care of the size of transistor and layout, try to reduce parasitic effect.

Owing to short connection between gate and drain, all NMOS FETs operate in saturation region, namely,

\[ V_{ds} = V_{os} = \sqrt{2I_dL/\mu C_{ox}W + V_{th}} \]  

(9)

According to the equation (8), it is clear that with a constant output current \( I_{out} \), the bigger \( W/L \) and then the smaller the threshold voltage is, the lower \( V_{s} \), and the higher the output dc voltage \( V_{out} \) is. However, the parasitic capacitor \( C_{sub} \) will increase and the dc output voltage will decrease if the area of transistor increases. So it is a tradeoff to increase the size of transistor. In the practical design, low threshold transistors [7] or nearly zero threshold transistors [4] are used.

C. The Body Effect and Ripple Voltage

If rectifiers use NMOS FET, the substrate bias voltage \( V_{os} \) (positive for n-channel devices) is equal to the voltage \( V_{t} (1 \leq i \leq N) \). The voltage across the reverse-biased source-substrate junction will increase the threshold voltage of the transistor. The bigger transistors’ subscript is, the higher the threshold voltage, and then the smaller voltage multiplier ability will increase. For those application, source and substrate voltage cancellation techniques [8] can be considered.

It should be noted that there will be a small ripple voltage, \( V_r \), at the output[3]. This ripple voltage is given by

\[ V_r = \frac{I_{out}}{f_{osc}C_{out}} = \frac{V_{out}}{f_{osc}R_{L}C_{out}} \]

(10)

The ripple voltage can be substantially reduced by increasing the operating frequency \( f_{osc} \) or using a large output capacitance \( C_{out} \). In the latter case, it would make the rectifier significantly longer to reach steady output state.

III. POWER DISSIPATION ANALYSIS

When \( V_d > V_{th} \), transistor is on. We assume that the drain-source voltage and the current holding time of every odd subscript transistor and even even subscript transistor are identical. And so their power consumption is.

Every even subscript transistor is on only for one half of input signal cycle with the condition of \( V_d > V_{th} \), that is, \( t \in \left[ -T_0, T_0 \right] \).

\[ T_0 = \frac{1}{\omega} \cdot \arccos \left( \frac{V_{out} + V_{th}}{2N} \right) \]

And so does every odd subscript transistor, the operating time is \( t \in \left[ T_0 + T_0, T_0 + T_0 \right] \).

The current from drain to source is

\[ I_s = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left( V_d - V_{th} \right)^2 = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left( V_{out}^2 + V_{th}^2 \right) \]

\[ = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left( V_{out}^2 + \left( \frac{V_{out} + V_{th}}{2} \right)^2 \right) \]

(10)

The dc current in each transistor, is also the dc current \( I_{out} \) in the output load, is given by

\[ I_{out} = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left( \frac{V_{out}^2}{2} + \left( \frac{V_{out} + V_{th}}{2} \right)^2 \right) \]

(11)

\[ P_d = \frac{1}{T} \int_{-T_0}^{T_0} V_d(t)I_s(t)dt \]

\[ = \frac{1}{T} \int_{-T_0}^{T_0} V_d(t)I_s(t)dt + \frac{1}{T} \int_{-T_0}^{T_0} V_d(t)I_s(t)dt \]

(12)

where \( T \) is the period of the input voltage signal, the first integral is the power dissipation of the transistor witch even subscript, and the latter is the power dissipation of the transistor with odd subscript. By solving the integral above with the expressions of \( V_d(t) \) and \( I_s(t) \), we get

\[ P_d = -\frac{2}{T} \left[ \frac{P_s}{2N} + \frac{K}{2} V_{th} \left( \frac{V_{out}^2}{2N} + V_{th} \right) \right] + \left[ \frac{\sin(\alpha T_0)}{12\pi} 4V_s^2 - 2 \left( \frac{V_{out}^2 + V_{th}}{2N} \right)^2 + \frac{9}{8} \left( \frac{V_{out}^2}{2N} + V_{th} \right)^2 \right] \]

(13)

Figure 4. The large signal equivalent model of diode-connected transistor.
where \[
K = \mu_c C_{ox} \frac{W}{L} \left( \sin(\phi \omega_T) = \frac{1}{V_T} \left[ V_{in}^2 - \left( \frac{V_{out}}{2N} \right)^2 \right] \right), \]
and \[
P_L = V_{out} I_{out} = \frac{1}{2} \mu_c C_{ox} \frac{W}{L} \left[ \frac{V_{in}^2}{2} + \left( \frac{V_{out}}{2N} + V_{th} \right)^2 \right] V_{out}.
\]
Neglecting substrate loss, the average input power \( P_o \) can be calculated by summing up the average power \( P_0 \) dissipated in each transistor and the power \( P_L \) required by the load. \( P_o \) is given by
\[
P_o = 2NP_0 + P_L - \frac{T}{T} \left[ K \left( V_{out} + 2N V_{th} \right) + \frac{\sin(\phi \omega_T)}{12\pi} \right] V_0^2.
\]
The power efficiency \( \eta \) is given by
\[
\eta = \frac{P_{out}}{P_o} = 1 - 2N \frac{P_0}{P_o}.
\]

IV. OPTIMIZATION ANALYSIS

For a voltage rectifier, the design parameters of rectifier are the size of transistor, the capacitance of coupling capacitor and storage capacitor and the number of stage. There are also some tradeoffs in the AC/DC RF rectifier design, such as the tradeoff between quality factor, power efficiency, the output voltage, the input impedance, operating point (load)[2] and the engineering feasibility of matched antenna. Optimization parameters include the number of stages, the size of Schottky diodes or transistor, the capacitance of coupling capacitors and energy storage capacitors.

As for the size of transistor, Large W/L will result in large saturation current, but, the reverse current will increase too. So, the output voltage will increase with the increase of W/L, however, the power efficiency is not the case. The output voltage and power efficiency are a function of W/L, shown in Fig 5(a) and Fig. 5(b).

When it comes to the number of stages. Owing to the body effect, the transistors’ threshold will increase, and the power efficiency of rectifier will decrease. So, the maximum power efficiency is obtained by using the minimum number of stages [9]. However, it is clear that the output voltage will be higher with more numbers of stages. And the simulation result is shown in Fig 6(a) and Fig. 6(b).

Therefore, considered the power efficiency, we should chose a proper number of stage and optimize the size of transistors.

V. CONCLUSION

This paper has introduced the operating principal of N-stage MOS FETs AC/DC rectifier with stray capacitance, body effect and ripple voltage considered. And the power dissipation and power efficiency for MOS AC/DC rectifier also presented in this paper. Furthermore, we also discussed design parameters optimization and some critical design tradeoffs in ultra low power rectifier design. The conclusion has been verified through elaborate simulation.

REFERENCES


