An Active-RC Complex Filter with Mixed Signal Tuning System for Low-IF Receiver

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Abstract—An active-RC complex filter synthesized from leapfrog low-pass prototype is proposed in this paper, which is less sensitive to components values variation compared with the common used cascade-pole method. Furthermore, a mixed-signal tuning system was implemented to make the RC time constant stable, and can be turned off after the completion of tuning. The filter was implemented in 0.18µm CMOS process. It is centered at 4MHz with 2MHz of bandwidth. It has the voltage gain of about -2dB, the image rejection ratio of about 28dB, the output 1-dB compression voltage of 0.39V, the in-band integral output noise of 32µVrms, and the power consumption of 6.1mW. The filter can be used in the low-IF GPS receiver.

I. INTRODUCTION

Complex filter is usually used in the low-IF wireless receiver to filter out the image signal, for its easy integration on chip. Active-RC filter is superior for the relatively large dynamic range compared with OTA-C filter. The common way to synthesize the active-RC complex filter is to connect the complex pole in series [1]-[3], but it is sensitive to the variation of the parameters like resistance and capacitance. This characteristic is similar to the cascade-biquad method for the real filter. A synthesis method based on leapfrog low-pass prototype is proposed here, and it is less sensitive to components values variation compare to cascade-biquad or cascade-poles method. The tuning system for the filter is based on the capacitor bank, and the tuning accuracy can be well-controlled by the bit number of the bank. Furthermore, the system can be turned off after the completion of tuning, and hence the power consumption of the tuning system can be considered as near zero.

II. SYNTHESIS OF THE COMPLEX FILTER

The complex filter can be considered as a single-band band-pass filter, which can be flatly shifted to the certain frequency from the low-pass prototype filter with the same bandwidth [1], as shown in Fig.1. If the center frequency is ωc, the image signal is therefore centered at −ωc, which can be rejected by the complex filter [1].

The architecture of the complex filter is shown in Fig.2. It consists of two same low-pass prototypes filters. The low-pass prototype is a third-order Butterworth leapfrog filter. The two low-pass filters can implement the complex filter by adding three groups of ‘frequency transform resistors’. The connections of these resistors are expressed by the node names rather than the wires for simplification. The synthesis principle is from the arithmetic offered by [4], and realized by the actual circuits here. The frequency transform resistors can be calculated as below

\[ R_i = \frac{1}{\omega_c C_i} \]  (1)

where \( \omega_c \) is the center frequency of the filter, \( C_i \) is the capacitance in the integrator section connected with the frequency transform resistors.

The values of the capacitors and resistors in the filter are also show in Fig.2. Comparing with the commonly used cascade-pole method for the synthesis of complex filter, this method (from leapfrog prototype) is superior as it is less sensitive to component variation. This can be verified by using the macro model of OPAMP in the system-level simulation.
III. OPAMP DESIGN FOR THE FILTER

Active-RC filter can usually achieve large dynamic range than OTA-C filter. However, the power consumption of active-RC filter may be large because of the large GBW of the OPAMPs in it. That is why it is very important to estimate the necessary GBW of the OPAMPs, and implement them with less power consumption.

A. Estimation for the GBW of the OPAMP

In order to estimate the necessary GBW for the OPAMP, an integrator (first order low-pass filter) cell is analyzed here, as shown in Fig.3.

If the OPAMP is ideal, that is, the gain and the bandwidth of the OPAMP is infinite, the transform function of the integrator is

$$H_i(s) = -\frac{R_2/(1/sC)}{R_i} = -A_c(s) \quad (2)$$

where $A_c(s)$ is defined as closed-loop gain.

If the OPAMP is not ideal, and its open-loop gain can be expressed as $A_o(s)$, then the transform function can be written as

$$H_o(s) = -\frac{R_2/(1/sC)}{R_i + R_2/(1/sC)A_o(s)}$$

$$= -\frac{A_c(s)}{1 + A_o(s)} \quad (3)$$

From (2) and (3), the transform function $H_o(s)$ warps from the ideal transform function $H_i(s)$. If the error between them can’t exceed $\delta$, then

$$A_o(s) \geq \left(\frac{A_c(s)}{\delta} - 1\right)\left[1 + A_c(s)\right] \quad (4)$$

If the bandwidth of the low-pass filter is $\omega_o$, the GBW of the OPAMP should satisfy

$$GBW \geq \left|\frac{A_c(j\omega)}{\delta} - 1\right|\left[1 + A_c(j\omega)\right] \cdot \omega_o \quad (5)$$

Equation (5) can be applied in estimating the necessary GBW of the OPAMP, when the passband of the filter has been set. In this design, the error in the passband should be within ±0.5dB, that is, within ±6%, besides, the highest gain of the integrators in the filter is 2, so that the necessary GBW can be calculated according to (5). The result is that the GBW should be about 100 times of the filter’s passband frequency.

The filter will work at 3MHz to 5MHz, so that the necessary GBW should be about 500MHz. Using the macro model of the OPAMPs, the system-level simulation shows the necessary GBW of the OPAMPs should be 460MHz, which is close to the estimation.

B. Implementation of the OPAMP

The implementation of the OPAMP is shown in Fig.4. It’s a typical two-stage miller-compensation OPAMP with common mode feedback circuit [5].
The simulation shows that the OPAMP can achieve GBW of 480MHz, phase margin of 70°, DC gain of 60dB, and power consumption of 1.1mW, with the load capacitor of 1.5pF and the load resistor of 10k ohm.

IV. TUNING SYSTEM

An important problem in integrated filter is the drift of the frequency characteristics like center frequency and bandwidth since the resistors and capacitors have different technology corners. In this design, a mixed signal tuning system based on capacitor bank is used to detect and compensate the drift of RC time constant. This kind of tuning principle has been applied in [6] [7]. Comparing with the former designs, this tuning system is easier to design and simper in timing issues, and can be turned off after the completion of tuning. The tuning accuracy of the tuning system is determined by the bit number of the capacitor bank, if the bit number is n, the tuning accuracy is 1/2^n. In the 5-bit system, the accuracy is about 3%.

Fig.5 shows the tuning system for the filter. The tuning system mainly composed by the integrator, the comparator and the digital part. The reference resistor should be chosen the same kind of resistor as the complex filter, and the capacitor bank should also be the same as the filter. The reference voltage Vref can be converted into current by the ‘constant-gm’ architecture.

The current is copied by the current mirror to charge the capacitor bank and this realise the function of an integrator. The integrator output voltage can be expressed as

$$V_o = \frac{V_{ref}}{t} \int$$

(6)

The integrator output is compared with the reference voltage of the comparator. If Vref>Vo, the comparator output is ‘1’, and the digital part increases the 5-bit tuning code of the capacitor bank till Vref<=Vo. If Vref<Vo, the comparator output is then ‘0’, and the digital part decreases the 5-bit tuning code till Vref>=Vo. This process makes Vo furthest close to Vref. After the comparison, Clk_dis will discharge the integrator voltage on the capacitor bank, while Clk_int gives the beginning signal to charge the capacitor bank when the new tuning code has been generated.

Fig.6 shows the digital part of the tuning system. The output signal of the comparator is sent into the encoder. The encoder changes the 1-bit signal to 5-bit code. If the output is ‘1’, then the 5-bit code is ‘00001’. If the output is ‘0’, then the 5-bit code is then ‘11111’, which is the complementary word of ‘-1’. In the next CLK2 cycle, the output of the counter will be changed and sent to the capacitor bank. The capacitance of the capacitor bank will change, so that the integrator will generate a new output voltage to compare with the reference voltage of the comparator. The process will repeat until the completion of tuning.
The tuning system can be turned off after the completion of tuning. In the 5-bit capacitor-bank tuning system, 2^5 cycles will be the longest time to tune the filter, so that the tuning can be turned off after 32 cycles. The latch-up signal will cut off the transistor between the "external Vdd" and the "internal Vdd" to turn off the tuning system. Meanwhile, the latch-up signal will restore the final tuning code in the latch to determine the final capacitance of the capacitor bank, as shown in Fig.5 and Fig.6.

V. EXPERIMENTAL RESULTS

This complex filter is designed for a low-IF GPS receiver. It was fabricated in the 0.18µm CMOS technology, and packaged in the QFN28. The chip area is about 3mm² including the filter and the tuning system. The chip layout is shown in Fig.7.

The input signals of complex filter are in four different phases, which are 0º, 180º, 90º and 270º respectively. The signals can be generated by the passive polyphase filter and/or closed-loop OPAMPs, but the four signals can’t match very well. Instead, the input signals are generated by ANDO VB8300 eight-channel baseband signal generator in this measurement.

The frequency characteristics of the complex filter is shown in Fig.8. The untuned filter is centered at 2.2MHz with the bandwidth of 1.1MHz, after tuning, the filter is then centered at 4.0MHz with the bandwidth of 2.1MHz, which meets the design purpose well. Besides, the image signal can be rejected about 28dB and the voltage gain in the passband is about -2dB. Furthermore, the in-band integral output noise is less than 32µVrms, and the 1-dB compression output voltage is about 0.39V. The output 1-dB compression dynamic range is therefore about 81dB.

The performance summary is show in Table.1, and it can be applied in the low-IF GPS receiver.

VI. CONCLUSION

A complex filter for low-IF GPS receiver has been discussed in this paper, this filter is more insensitive than the common used cascade-pole complex filter, for it’s directly synthesized from the leapfrog low-pass filter. This filter has achieved the image rejection ratio of 28dB and dynamic range of 58dB, with 6.1mW of power consumption. Besides, the tuning system has been verified accurate for this filter.

REFERENCES