A Robust Novel Technique for SPICE Simulation of ESD Snapback Characteristic

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Abstract
This paper presents a robust and novel technique for the circuit simulation of ESD (ElectroStatic Discharge) snapback characteristic. A new linearization scheme for the avalanche current model in ESD evaluation shows a good convergence behavior during ESD stress simulation. This technique is compatible with the traditional circuit simulator based on the modified nodal analysis (MNA) like SPICE. We have implemented a simple ESD MOSFET model in SPICE3f5, and the simulation results are discussed.

1. Introduction
The ESD protection circuitry is an indispensable part of IC design. When MOSFETs are used as ESD protection devices, several ESD models ([2], [3], [5]) have been developed for circuit simulation. These models have been implemented in SPICE as sub-circuits in user-input netlists or as integrated code modules in simulator’s source program. Because ESD MOSFETs show the snapback behavior in their I-V characteristics, these models usually cause convergence problems in circuit simulation.

For the numerical instability caused by circuits having ESD MOSFETs, the matrix singularity is the most often encountered problem due to the snapback behavior of these devices. At the turning point for the negative differential resistance (NDR) region, the differential conductance of the device becomes infinite, leading to the singular circuit (Jacobian) matrix. Another problem is the SPICE runtime error: “time step too small”, which often occurs during the transient analysis of ESD circuits. This is also caused by the device snapback effect. Since SPICE uses voltage as its primary independent variables, when simulation steps to the vicinity of turning point, simulator may jump between more than one possible solutions and fails to converge.

In this paper we present an algorithm and discuss its implementation for a simple ESD MOSFET model. The technique is based on the algorithm in [4], which is proposed to handle two-terminal resistors whose I-V characteristics are described by a function with a single-point singularity [4]. Because branch voltage and branch current both are independent variables, so they no longer satisfy the relation \( i = f (v) \) after matrix solving. While introducing the branch current \( i_b \) as independent variable, we have the option of choosing either the branch voltage \( v_b^{(k)} \) or branch current \( i_b^{(k)} \) for the last iteration as initial value to calculate the differential conductance through the equation

\[
g^{(k)} = \frac{dv}{i_b^{(k)}}
\]  

or

\[
g^{(k)} = \frac{dv}{v_b^{(k)}}
\]

Where \( k \) denotes the \( k^{th} \) iteration, \( v^{(k)} \) and \( i_b^{(k)} \) represent the branch voltage and branch current value after the \( (k-1)^{th} \) iteration.

2.2 Breaking the Feedback Loop
Fig. 1 shows the simple ESD snapback model for ggNMOS (gate-grounded NMOS). There are three resistors, one diode, and one dependent current source in this model. The diode and dependent current source can be described as follows

\[
i_b = I_s \left( \exp \left( \frac{V_{BS}}{V_T} \right) - 1 \right)
\]

\[
i_{sym} = (M - 1) \beta i_b
\]

\[
M = \exp \left( k \left( v_{DB} - v_i \right) \right) - \exp \left( k \left( -v_i \right) \right) + 1
\]
Where $i_b$ is the conventional diode model, $i_{gen}$ is controlled by $i_b$ and $v_{DB}$, $M$ is the multiplication factor. $\beta$, $k$ and $v_1$ are all fitting parameters.

The occurrence of the snapback is physically due to a positive feedback process and happens in a very short period of time. Suppose that at the initial condition, the voltages $v_{DS}$ is set to zero, then $v_{DS}$ and $v_{GS}$ are all zeros. As the voltage $v_{DS}$ rises, so do $v_{DS}$ and $v_{GS}$. At the same time $i_b$ and $i_{gen}$ rise. The rising of $i_{gen}$ pushes $v_{GS}$ rise further more, causing $i_b$ and $i_{gen}$ rise still further. Thus, the above chain of actions form a positive feedback loop. To improve the convergence, we cut off this feedback loop by making the dependent current source $i_{gen}$ independent upon $i_b$ when filling up the stamp entries. In the conventional SPICE evaluation step, for the dependent current source $i_{gen}$, $\partial i_{gen}/\partial v_{DS}$ and $\partial i_{gen}/\partial i_b$ should be calculated and fill into the stamp. To break the positive feedback loop formed by $i_b$ and $i_{gen}$, $\partial i_{gen}/\partial i_b$ is proposed to set to zero. Then in the whole circuit stamp, $i_{gen}$ reduces to a non-linear resistor with 1-V characteristics like a diode, which guarantees the matrix away from singularity.

The second part of this algorithm is the standard way of computing the stamp entries by iterations in updating the nodal voltage. The third part is the current iteration introduced by [4]. This step insures that the system of equations is guaranteed to represent a feasible physical operation condition regardless of the results of the previous iteration. This technique is also used in the fifth part. The fourth part is the newly proposed approach for breaking the positive feedback process. When computing $g_{gen}(k)$, $i_b$ is updated as $i_b(k)$ and is assumed to be a constant by setting $\partial i_{gen}/\partial i_b = 0$. This makes $i_{gen}$ be independent of $i_b$ in the iteration step, and then $i_{gen}$ becomes a non-linear resistor whose I-V characteristic can be described by a function with a single-point singularity. When calculate $i_{gen}(k)$ or $v_{DB}(k)$, $i_b$ is also updated as $i_b(k)$ which guarantees that the results for nodal voltages and branch currents still satisfy the system of equations.

### 3. Simulation Results

To validate the new linearization technique, we first compare the results of the current source driven DC analysis using both the new model implementation and the sub-circuit model implementation for the simple MOSFET model. The two simulation results matched very well which shows that the new model implementation has a very good accuracy.

The transient analysis is the most challenging simulation for ESD models. The previous simple ESD model as well as other models ([2], [3]), if used as sub-circuit in SPICE input file, or implemented as an integrated part of SPICE source code using conventional linearization method, always encounter the “time step too small” problem during the transient analysis. After using the new linearization technique, the transient simulation converges quickly.

![Simple ESD snapback model](image1)

**Fig. 1** Simple ESD snapback model

**2.3 Implementation of this ESD model**

In Fig. 1, there are four nodal voltages $v_D$, $v_F$, $v_B$ and $v_S$ declared as variables, and two currents $i_{gen}$ and $i_b$ are also declared as variables. The algorithm works as follows:

1. Declaring currents $i_{gen}$ and $i_b$ as independent variables.
2. If $v_{BS}(k)$ is physically admissible, we calculate the stamp entries $g_b(k)$ and $i_b(k)$ according to (1) and (3).
3. Otherwise using equation (2) to compute $g_b(k)$ and $i_b(k) = i_{gen}(k)$.
4. If $v_{DB}(k)$ is physically admissible, then use equation (1) and (4) to calculate $g_{gen}(k)$ and $i_{gen}(k)$, whereas $i_b = i_b(k)$ and setting $\partial i_{gen}/\partial i_b = 0$.
5. Otherwise using equation (2) to calculate $g_{gen}(k)$ and $i_{gen} = i_{gen}(k)$, whereas $i_b = i_b(k)$ and setting $\partial i_{gen}/\partial i_b = 0$.
time. At the beginning of the simulation, the ESD device is off. And then the voltage drop increases as the source voltage rises. When the voltage increases to a level where the ESD device snapbacks, the voltage drop reduces to the holding voltage quickly. As the source voltage continues to rise, however, the current flow through the ESD device increases and the voltage drop on the ESD device increases. While the source voltage ramps down, the voltage drop on the ESD device decreases slowly, because of the small on resistance of the ESD device. At the holding point, the reduction of current can cause the voltage drop on the ESD device to increase because of the negative differential resistance. However, because the ESD device consumes not supplies power, the increased voltage drop on ESD device will never exceed the voltage source.

4. Conclusion
We have proposed a new linearization technique, which is used to implement a simple ESD MOSFET model (ggNMOS). The current-source driven DC analysis is used to validate the robustness of this technique. Also ramp-up-ramp-down transient analysis and HBM model simulation are used as test cases. All tests show the good convergence property of this new technique. This technique can be used to implement other ESD models, which have similar characteristics with our simple ESD model.

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